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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/605,408	09/29/2003	Kern Rim	YOR920000707US2	2407

27127 7590 06/13/2006

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EXAMINER	
MITCHELL, JAMES M	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 06/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/605,408	RIM, KERN	
	Examiner	Art Unit	
	James M. Mitchell	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 February 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to applicant's request for continued examination filed February 8, 2006.

Declaration

The 1.131 declarations filed on April 21, 2006 under 37 CFR 1.131 has been considered but is ineffective to establish priority before February 7, 2002.

The evidence submitted is insufficient to establish either conception or due diligence prior to the critical date. The affidavit or declaration and exhibits must clearly explain which facts or data applicant is relying on to show completion of his or her invention prior to the particular date. Vague and general statements in broad terms about what the exhibits describe along with a general assertion that the exhibits describe a reduction to practice "amounts essentially to mere pleading, unsupported by proof or a showing of facts" and, thus, does not satisfy the requirements of 37 CFR 1.131(b). In re Borkowski, 505 F.2d 713, 184 USPQ 29 (CCPA 1974). Applicant must give a clear explanation of the exhibits pointing out exactly what facts are established and relied on by applicant. 505 F.2d at 718-19, 184 USPQ at 33. See M.P.E.P section 715.07 [R-3].

While applicant provided copies of an e-mail, and summarized what they related to, none of the e-mails when looking at the record as a whole corroborated the claimed method. The most relevant e-mail found in Exhibit D, stated generally "Leathen finished bonding, grinding…the strained Si-directly on –insulator;" this does not corroborate the

claimed invention since it fails to even mention most of the claimed steps or establish its use. Moreover, grinding is not even a claimed step.

In addition, even assuming that conception has been established applicant has made no reference toward diligence[1] that is needed to establish priority. For the reasons stated supra, the declaration is found ineffective.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-23 are rejected under 35 U.S.C. 102(e) as being anticipated by Currie (U.S. 2006/0014366).

Currie (Fig. 2A-8A) disclose:

(cl. 1, 13) A method of forming a strained silicon-on-insulator structure, the method comprising the steps of: forming a silicon layer (118; Par. 0051) on a strain-inducing layer ("SiGe"; Par. 0047)[2] so as to form a multilayer structure (Fig. 2A), the strain-inducing layer having a different lattice constant than silicon so that the silicon layer is

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[1] Requested in office action filed August 8, 2005.
[2] Same material as claimed

strained during the forming step ("epitaxial growth"; Par. 0050) as a result of a lattice mismatch with the strain-inducing layer, and then bonding the multilayer structure to a substrate (154, Fig. 4) the bonding step being chosen from the group consisting of directly bonding a first insulating on (Par. 0059) and contacting the strained layer silicon layer of the multilayer substrate to a second insulating layer (152) on the substrate (154), the strained silicon layer (118) directly contacting the insulating region (152); and then removing the strain-inducing layer (Fig. 4-6; Par. 0062) to expose a surface of the strained silicon layer and to yield a strained silicon-on-insulator structure (Fig. 6) comprising the substrate (154), the insulating region (152), and the strained silicon layer (118) on the insulating region;

(cl. 2, 9) wherein the substrate is formed of a semiconductor material (Par. 0059);

(cl. 3, 23) wherein the strain-inducing layer is formed of a SiGe alloy, and the strained silicon layer is under tensile strain (CLAIM 21 of Currie; see also footnote 2);

(cl. 4) wherein the strained silicon layer (118) is formed by epitaxial growth on the strain-inducing layer (Par. 0050);

(cl. 5, 10, 14) the strain inducing layer is SiGe alloy (e.g. metal-semiconductor; Par. 0047) wherein the removing step comprises preferentially etching the strain-inducing layer with hydrofluoric acid (Par. 0062);

(cl. 6, 15) wherein the bonding step comprises directly bonding the first insulating layer on the strained silicon layer of the multilayer substrate to the second insulating layer on the substrate (Par.0059);

(cl. 7, 16) the bonding step comprises directly bonding the insulating layer on and

contacting the strained silicon layer of the multilayer substrate to the semiconductor layer of the substrate (Par. 0062);

(cl. 8, 17) wherein the bonding step comprises directly bonding the first semiconductor layer of the substrate to the second semiconductor layer (Par. 0057) of the multilayer substrate and separated from the strained silicon layer by the insulating layer (152);

(cl. 11, cont. cl. 13) further comprising the step of forming an IC device (Fig. 8A), in the surface of the strained silicon laver;

(cl. 12, 19) the step of forming the IC device , comprises the steps of forming source and drain regions (214,216), in the surface of the strained silicon layer (118) so that the strained silicon layer defines a channel between the source region, and the drain region, the channel being in direct contact with the insulating layer (152);

(cl. 18) the removing step comprises one or more techniques chosen from the group consisting of wafer cleaving (Par. 0064);

(cl. 20) forming a gate electrode (212) separated from channel by insulating region (210);

(cl. 21) forming a gate oxide (210) on the surface of the strained silicon layer, and forming gate (212) on the oxide.

(cl. 22) using the semiconductor layer (Par. 0072) to form a first gate electrode separated from the channel by the insulating region; forming a gate oxide (e.g. 210) on the surface of the strained silicon layer (118) and ; forming a second gate electrode on the gate oxide (Fig. 20);

Response to Arguments

Applicant's arguments with respect to claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James M. Mitchell whose telephone number is (571) 272-1931. The examiner can normally be reached on M-F 8:00-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jmm

CARL WHITEHEAD, JR.
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

June 9, 2006